Rockwell

# PARALLEL PROCESSING SYSTEM (PPS)
# DATA SHEET

## ROM/RAM/IO A17XX



### DESCRIPTION

Rockwell introduces two new microcomputer circuit devices which provide a flexible system for cost sensitive applications. The two circuits comprise a CPU chip (P/N 11660 described in data sheet Number 29000 D02) and a combination Memory and I/O chip (described in this data sheet). These chips may be used as a complete two chip microprocessor or with other Rockwell circuits of the PPS-4 family to provide a broad spectrum of system functions at lower costs than previously attainable.

The PPS-4/2 System has been designed to provide a basic two circuit microcomputer which is optimized for applications requiring low cost and high performance. The two circuits provide all the computing power and applications flexibility which would require five or more of the conventional PPS-4 circuits to implement. The PPS-4/2 may be expanded to more complex applications by using any of the large family of PPS-4 circuits so that the cost of more complex systems may be reduced. The Memory/IO Circuit has a full 2K bytes of program storage in ROM and 128 x 4-bit words of data storage in RAM. This circuit also includes an input/output capability which allows the individual control of 16 one-bit I/O ports. All of the functions in the Memory/IO Circuit make common usage of the address decoding circuitry.

#### READ-ONLY-MEMORY (ROM) SECTION

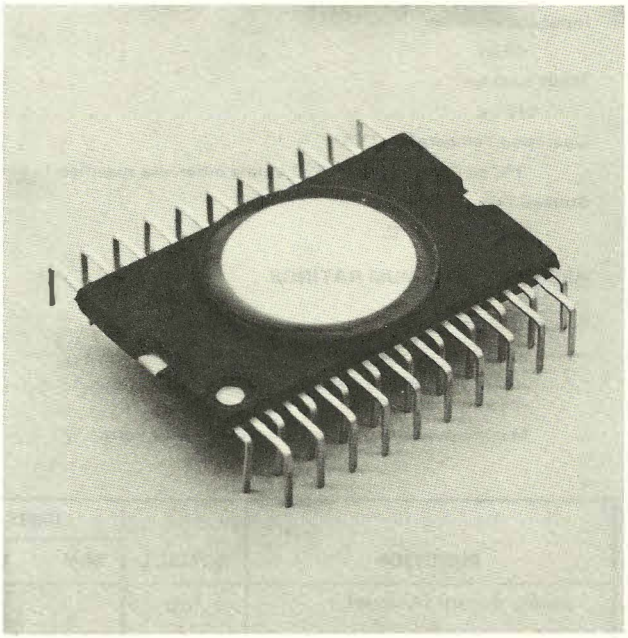
The Read-Only-Memory is addressed in the same manner as the PPS-4 during phase 2 time, by a combination of the eleven address bits brought into the circuit and the matching of either a "1" or a "0" on the ROM/RAM Select (RRSEL) pin and an internal code established in the ROM pattern. In effect the RRSEL signal may be used as a twelfth address bit or may be used to "bank select" additional ROM's beyond the 4K direct addressing capability of the 12-bit address bus.

#### DATA MEMORY (RAM) SECTION

The Data Memory is addressed during phase 4 time. In this circuit the state of the RRSEL during phase 4 (the internal code established during fabrication), and the A/B 8 signal will establish if the RAM in the memory circuit is being accessed. Both the A/B 8 signal and the RRSEL signal must match the internal code to select the RAM. The lower 7-bits of the address will then establish which 4-bit word is being accessed and the WI/O line performs the same function as in the PPS-4 to signal that a read or a read and simultaneous write is being commanded.

#### INPUT/OUTPUT SECTION

In the Memory/IO Circuit, the input/output section is commanded by the same technique used by all PPS-4 I/O devices. First an IOL instruction is executed in the CPU which causes the WI/O line to signal all I/O devices in the system that the next instruction byte contains a device identification (4-bits) and the specific command to be executed (4-bits). The IOL instruction, via the WI/O line, also tells the RAM to stay off the data bus so that the input/output data may be transmitted.

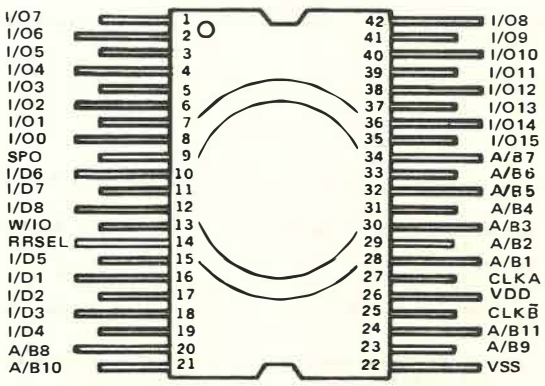


In this circuit the I/O section may be encoded during fabrication to be identified as device 0, 2, 4, or 6 so that any conflict with other I/O device addresses used in the specific system may be avoided.

The SPO signal generated when power comes on causes the enable flip-flop to be set to zero so that all 16 I/O ports are floated. The individual holding flip-flops are not set automatically.

### FEATURES

- 2048 x 8 Read-only Program Memory (ROM)
- 128 x 4 Data Memory (RAM)
- 16 One-bit Input/Output Ports
- Option of Using Two Memory/IO Circuits per System




**A17XX ROM/RAM/IO Pin Configurations**



Specifications subject to change without notice
Revision 2, Oct. 1976

# SPECIFICATIONS

## OPERATING CHARACTERISTICS

Supply Voltage:

VDD = -17 Volts ±5%
(Logic "1" = most negative voltage $V_{IL}$ and $V_{OL}$.)

VSS = 0 Volts (Gnd.)
(Logic "0" = most positive voltage $V_{IH}$ and $V_{OH}$.)

System Operating Frequency:

199 kHz

Device Power Consumption:

500 mw

Input Capacitance:

<5 pf

Input Leakage:

<10 ua

Operating Temperature (TA):

0°C to 70°C. (TA = 25°C unless otherwise specified.)

Storage Temperature:

-55°C to 120°C.

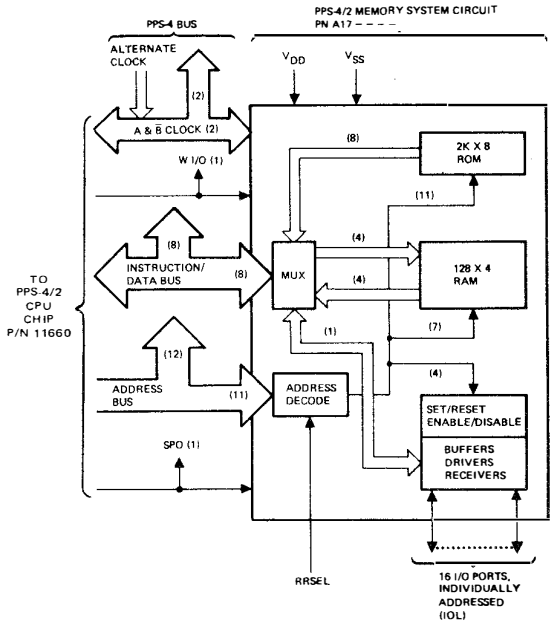
## ABSOLUTE MAXIMUM RATINGS

Supply Voltage

|VDD-VSS| = 27 volts maximum.

Input Voltage with respect to VSS
-27 volts maximum.

Maximum positive voltage on any pin +0.3 volts.




**A17XX Simplified Block Diagram**

| FUNCTION | | SYMBOL | LIMITS (VSS = 0V) MIN | TYP | MAX | LIMITS (VSS = +5V) MIN | TYP | MAX | UNIT | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply Current (Average) | | $I_{DD}$ | | 20 | 28 | | 20 | 28 | mA | VDD = -17.85V<br>VSS = 0V<br>F = 199 kHz<br>$T_A$ = 25°C |
| Input and Output Characteristics — System Bus | | | | | | | | | | VDD = -17V ±5%<br>VSS = 0V |
| $I/D_{1,5,6-8}$ | $A/B_{1-11}$ W/IO RRSEL | $V_{IH}$<br>$V_{IL}$ | -1.5<br>-6.5 | | +0.3<br>-17.85 | +3.5<br>-1.5 | | +5.3<br>-12.85 | V<br>V | |
| | $I/D_{2-4}$ | $V_{OH}$<br>$V_{OL}$ | -1.0<br>-7.5 | | +0.3<br>-17.85 | +4.0<br>-2.5 | | +5.3<br>-12.85 | V<br>V | |
| SPO | | $V_{IH}$<br>$V_{IL}$ | -1.0<br>-7.5 | | +0.3<br>-17.85 | +4.0<br>-2.5 | | +5.3<br>-12.85 | V<br>V | OR |
| CLKA<br>CLKB | | $V_{IH}$<br>$V_{IL}$ | -0.5<br>-10.0 | | +0.3<br>-17.85 | +4.5<br>-5.0 | | +5.3<br>-12.85 | V<br>V | |
| | | | | | | | | | | |
| $I/O_{0-15}$ | | $V_{IH}$<br>$V_{IL}$ | -1.0<br>-4.2 | | +0.3<br>-17.85 | +4.0<br>+0.8 | | +5.3<br>-12.85 | V<br>V | |
| | | $V_{OH}$<br>$V_{OL}$ | NOTE 1<br>floating(≥5M) | | | NOTE 1<br>floating (≥5M) | | | Ω | VDD = -12V ±5%<br>VSS = +5V ±5% |

NOTE: 1. Output driven to VSS with maximum "ON" resistance ($RON_{MAX}$) of 1 0K ohms and maximum drive current ($I_{MAX}$) of 2.7 ma.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